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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2416	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/621,060	HAALEN ET AL.	
	Examiner	Art Unit	
	IAN N. MOORE	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 6, filed 3-27-09, with respect to 35 U.S.C. 112, first paragraph have been fully considered and are persuasive. In particular, **the applicant stated on the record that** the claimed invention "*allow less of a number of bits to be forwarded than were transmitted"* is disclosed as "*data packets 1, 2, 3, 4 were originally transmitted, however, only data packet packets 1, 3, 4 arrives at destination B*". **The application also admits that the invention is well known in the art since** "There is no experimentation required by the average individual because an artisan of ordinary skill in the art would easily comprehend the above-referenced disclosure. Without a reasonable basics of questioning the adequacy of disclosure to enable a person of ordinary skill in the art to make and use the claimed invention". Thus, the rejection of claims 1-16 under 35 U.S.C. 112, first paragraph has been withdrawn.

2. Applicant's arguments with respect to claims 1-16, under prior art and double patenting rejections have been considered but are moot in view of the new ground(s) of rejection.

Regarding claims 1-16 on double patenting rejections, the applicant stated that, "…applicants thank the examiner for deferring the double patenting rejection until all other grounds of rejection are overcome …." on page 7-8.

In response, examiner acknowledges the applicant remarks accordingly the double patenting rejection is sustained.

Regarding claims 1, 6, 11, the applicant argued that, "…Boduch fails to teach or suggest … "*said data packets are discarded or accepted depending on the source from which the data packet originates"*… as exampled among other places in the applicant Fig. 10, wherein

cells 1, 3 and 4 are forwarded, and cell 2 is discarded with destination B not receiving a copy of a cell; thereby allowing less of a number of bits to be forwarded than were transmitted...." in pages 8-9.

In response to applicant's argument, t**he examiner respectfully disagrees** with the argument above.

Boduch discloses the switch configured to discard or accept data packets depends on the source from which the data packet originate (**see FIG. 1, 2, discarding or transmitting/accepting packets/cells based/depends on the source/originator (*where the packets/cells originate*) (i.e. based on the source/originator who transmit a sequence number and identification number of the packet/cell which is used for discarding/transmitting; see col. 5, line 9-30, 50-65; see col. 6, line 30-60; see col. 8, line 40-50**).

Boduch discloses wherein in response to a data packet being received out of order at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets out of sequence at the first receive/input interface 111; see col. 5, line 60 to col. 6, line 7), data packets received at the first input port are discarded for a period of time (see FIG. 2, sequence manager of AISC 110 drops the packet/cell, (e.g. by not writing into FIFO 204, or determining as bad cell), for that period of time; see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40) while data packets received at the other input ports are processed (see FIG. 1,2, while/when receiving packets/cells at the second receive/input interface 112 by writing them into FIFO 204 for transmission; see col. 6, line 20-29,60 to col. 7, line 5, see col. 7, line 20-30; see col. 10, line 32 to col. 11, line 6) such that the data packets forwarded on the output are in correct order (see FIG. 1,2, so that

packets/cells transmitted from the cell selector 206 at output/transmit interface of ASIC 100 is sequential order; see col. 10, line 32 to col. 11, line 6), and further allow less of a number of bits to be forwarded than were transmitted (**see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40; allowing/selecting best copy of cell bits (note that ATM cell is 53 bytes/424 bits) for forwarding at the output/transmit interface than transmitted from input interface by discarding/dropping "not receiving" bad/out-of-sequence/copied cell bits thereby allowing/selecting the less number of cell bits to be transmitted**; in other word, discarding cause the less number of cells/bits to be forwarded/allowed/selected than originally transmitted packets).

Identical to applicant broadly claimed invention, Boduch discloses sending/transmitting sequential packets/cells from the send/transmitter, discarding the out-of-sequence packet/cell, then forwarding the resulted number of packets/cells, and thus the forwarded number of packets/cells/bits are lesser number of packets/cells/bits that transmitted. This scenario is also well known and established in the art as admitted by the applicant. Since the claimed functionality disclosed in the specification and admitted by the applicant is identical to the functionality of the commonly known prior art clearly disclosed by Boduch.

Regarding claims 1-16, the applicant argued that, "…the office action failed to establish a prima facie case of obviousness because the combination of Almay and Soirinsuo fails to teach or suggest all the claim elements... Soirinsuo never allows data at any more than input port to be consider, or "processed" at any given time…Even though Soirinsuo mention the word "discard", the applicant respectfully maintain that the art distinctly teach away from

"discard". Soirinsuo does not mention any provision for actually detecting if packets are cells are being received out of order or not... it is not even possible for Soirinsuo to specifically respond "to a commonly sourced data packet being received out of order" by any means… Soirinsuo in fact teaches away form the claim element…" in pages 10-11.

In response to applicant's argument, t**he examiner respectfully disagrees** with the argument above since the combined system of Almay and Soirinsuo as detailed below.

Almay discloses the switch configured to perform processing data packet depending on the source from which the data packets originate (**see FIG. 1, Node B performing processing of packets depending/based on the source node A, where node A transmits packet at different time or Node A transmit re-route notification; see col. 3, line 1-60**); wherein in response to a data packet being received at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20), data packets received at the first input port are wait/hold for a period of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for predetermined period) while data packets received at the other input ports are processed (see FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60) such that the data packets forwarded on the output are in correct order (see FIG. 1, routing the received packet in a correct/proper order (i.e. note that a correct/proper order of packets is formed when nodes A and B deactivating the route a-b for a predetermined time then activating the route A-B) via an output interface of node B; see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50), thereby allowing less of a number of bits to be forwarded than were transmitted (see col. 9, line 20-45; see col. 10, line 10-30;

allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time).

Soirinsuo discloses the switch configured to discard or accept data packet depending on the source from which the data packets originate (**see FIG. 8, 9, 11, discarding or forwarding packets/cells depends/based on the originator/source switch who sends packets with last cell indication set (i.e. AUU or signaling) with associated cell identification VPI/VCI; last cell indication set cause the switchover to discard, non-last cell indication does not cause the switchover; see col. 9, line 1-30, 50-65; see col. 10, line 5-25**); wherein in response to a data packet being received out of order at a first of the plurality input ports (see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the first normal input port of 1104; see col. 9, line 20-35), data packets received at the first input port are discarded for a period of time (see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the first/normal/old channel port 1104 are discarded during switch-over interval/time) while data packets received at the other input ports are processed (see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new channel port), such that the data packets forwarded on the output are in correct packet order (see FIG. 8, 11, the packets/cells are transmitted/forwarded on the output channel port 1106 in the same proper/accurate order (i.e. the order as if the packets/cells are not lost due to failure/congestion); see col. 9, line 20-35; see col. 10, line 29-46) and further allow less of a number of bits to be forwarded than were transmitted (see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of

cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time).

In response to augment on Soirinsuo, Soirinsuo's teaches the switch determines whether or not to discard the packet based upon the transmitter/sender/source where the cells originate, where the transmitter/sender/source uses the AUU or user signaling bit to set the indication of the last cell. Based on that cell with the AUU set, the switch-over occurs which triggers the discarding of cells as set forth above. Thus, it is clear that Soirinsuo teaches the amended limitation.

Examiner acknowledges the applicant admission of Soirinsuo reciting the text and invention of "discarding". Since Soirinsuo clearly and precisely discloses the text for utilizing "**discarding**" in the invention as admitted by the applicant, Soirinsuo does not teach away from "discard". Moreover, since **the exact claimed limitation "discarding"** is being disclosed in Soirinsuo, one skilled in the ordinary would clearly see that Soirinsuo clearly does not teach away.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the rejection is based on the combined system of Almay and Soirinsuo clearly teach the broadly claimed invention.

In view of the above, it is clear that the cited prior arts still disclose the applicant broadly claimed invention as detail in the rejection below.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-4, 6-9, and 11-16 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,370,112 (hereinafter refers to as Voelker) in view of Almay (US 5,809,011).

Regarding claim 1, Voelker discloses a communication network comprising (see Voelker claim 1, lines 1-5):

at least two mutually different routing paths for commonly sourcing data packets (see Voelker claim 1, step a-c);

the switch having a plurality of inputs respectively coupled to the routing paths for receiving the data packets, and an output for forwarding the data packets (see, claim 1, step a-d);

the switch configured to discard or accept data packets depends on the source form which the data packet originate (**see claim 1, step e; discarding or transmitting/accepting packets depends on the source, by means of marker packet, from which data packet originated**);

wherein in response to a data packet being received out of order at a first of the plurality inputs, data packets received at the first input are discarded for a period of time while commonly sourced data packets received at the other inputs are processed such that the data packets forwarded on the output are in correct packet order (see claim 1, steps e-g).

Voelker does not explicitly disclose "ports" and "allow less of a number of bits to be forwarded than were transmitted".

However, Almay teaches at least two mutually different routing paths for commonly sourcing data packets (see FIG. 1, first path 105-111 and second path 106-112 for common source cells 103; see col. 3, line 36-67);

a switch (see FIG. 1, 2, Cell stream alignment best cell copy selection ASIC 100) having a plurality of inputs (see FIG. 1, received/input interfaces for paths 105-111 and 106-112) respectively coupled to the routing paths for receiving the data packets (see FIG. 1, coupling to paths 105-111 and 106-112 for receiving packets/cells; see col. 4, line 1-40,44-53), and an output for forwarding the data packets (see FIG. 1, transmit/output interface of ASIC 100 for transmitting/forwarding the packets/cells; see col. 4, line 1-40,44-53);

wherein in response to a data packet being received out of order at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets out of sequence at the first receive/input interface 111; see col. 5, line 60 to col. 6, line 7), data packets received at the first input port are discarded for a period of time (see FIG. 2, sequence manager of AISC 110 drops the packet/cell,

(e.g. by not writing into FIFO 204, or determining as bad cell), for that period of time; see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40) while data packets received at the other input ports are processed (see FIG. 1,2, while/when receiving packets/cells at the second receive/input interface 112 by writing them into FIFO 204 for transmission; see col. 6, line 20-29,60 to col. 7, line 5, see col. 7, line 20-30; see col. 10, line 32 to col. 11, line 6) such that the data packets forwarded on the output are in correct order (see FIG. 1,2, so that packets/cells transmitted from the cell selector 206 at output/transmit interface of ASIC 100 is sequential order; see col. 10, line 32 to col. 11, line 6), and further allow less of a number of bits to be forwarded than were transmitted **(see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “ports” and “allow less of a number of bits to be forwarded than were transmitted", as taught by Almay in the system of Voelker, so that it would minimum loss of data; see Almay col. 1, line 45-50.

Regarding Claim 2, Voelker discloses response to a commonly sourced data packet being received out of order at a second of the plurality inputs, commonly sourced data packets received at all of the inputs are discarded for a period of time (see Voelker claim 1, step e-g). Almay discloses in response to a commonly sourced data packet being received at a second of the plurality input ports (see FIG. 2, when receiving packets/cells at the second interface A-B;

see col. 3, line 1-60), commonly sourced data packets received at all of the input ports are hold/wait for a period of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing packets/cells at the first interface a-b or other interfaces (since ATM node can have more than two interfaces, see Almay col. 5, line 1-16; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20).

Regarding Claim 3, Voelker discloses the period of time lasts until fill-the switch is informed that re-ordering of the commonly sourced data packets is no longer possible (see Voelker claim 1, 4). Almay discloses the period of time lasts until the switch is informed that re-ordering of the commonly sourced data packets is no longer possible (see col. 3, line 1-50; predefined period is defined such that ordering of packets at the new route connection that transmit cells/packets from possible and not disrupted. Since the predefined time last until the "ordering" of packet is "possible/not-disrupted", and thus "re-ordering" of packets are "not possible/disrupted").

Regarding Claim 4, Voelker discloses the period of time has a predetermined length of time (see Voelker, claim 1-4). Almay discloses the period of time has a predetermined length of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing packets/cells from subscriber A at the first interface a-b for predetermined period).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide ports, as taught by Almay in the system of Voelker, so that it would minimum loss of data; see Almay col. 1, line 45-50.

Regarding claim 6, a switch for use in a communication network the switch receiving data packets having a packet order, determining whether the received data packets are in correct

order, and forwarding the received data packets in correct packet order, the switch comprising (see Voelker, claim 1, lines 1-4, steps a-c):

at least two incoming/inputs for receiving the data packets via respective routing paths and an output for forwarding data packets (see Voelker, claim 1, steps a-d);

said data packets are discarded or accepted depending on the source form which the data packet originate (**see claim 1, step e; discarding or transmitting/accepting packets depends on the source, by means of marker packet, from which data packet originated**);

originating from the source, wherein in response to a commonly sourced data packet being received out of order at a first of the plurality inputs, commonly sourced data packets received at the first input port are discarded for a period of time while commonly sourced data packets received at the other inputs are processed (see Voelker, claim 1, steps e-g).

Voelker does not explicitly disclose "ports" and "allow less of a number of bits to be forwarded than were transmitted".

However, Almay discloses at least two incoming ports for receiving the data packets (see FIG. 1, two input interfaces to Node B receiving packets) via respective routing paths (see FIG. 1, via different/separate paths a-b and A-B; see col. 2, line 33-67; see col. 4, line 20-35) and an output port for forwarding data packets (see FIG. 1, 3, and output interface of Node B for routing packets; col. 2, line 56 to col. 3, line 50);

wherein in response to a commonly sourced data packet being received at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20), commonly sourced data packets received at the first input port are wait/hold for a period of time (see FIG. 2, col. 2,

line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for predetermined period) while commonly sourced data packets received at the other input ports are processed (see FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60), thereby allowing less of a number of bits to be forwarded than were transmitted (**see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "ports and allowing less of a number of bits to be forwarded than were transmitted", as taught by Almay in the system of Voelker, so that it would minimum loss of data; see Almay col. 1, line 45-50.

Regarding Claim 7, the claim, which has disclosed all the limitations of the respective claim 2. Therefore, it is subjected to the same rejection as set forth above in claim 2.

Regarding Claim 8, the claim, which has disclosed all the limitations of the respective claim 3. Therefore, it is subjected to the same rejection as set forth above in claim 3.

Regarding Claim 9, the claim, which has disclosed all the limitations of the respective claim 4. Therefore, it is subjected to the same rejection as set forth above in claim 4.

Regarding claim 11, a switch configured for receiving data packets having a packet order, determining whether the received data packets are in correct order, and forwarding the received data packets in correct packet order, comprising (see Voelker, claim 1, lines 1-5):

a plurality of inputs for successively receiving said data packets from a respective plurality of routing paths (see Voelker claim 1, steps a-d); and

an output for forwarding data packets (see Voelker claim 1, steps a-d);

said data packets are discarded or accepted depending on the source form which the data packet originate (**see claim 1, step e; discarding or transmitting/accepting packets depends on the source, by means of marker packet, from which data packet originated**);

wherein in response to a data packet being received out of order at a first of any one of the plurality inputs, data packets are discarded for a period of time at the first input while being allowed at the other inputs (see Voelker claim 1, steps e-g).

Voelker does not explicitly disclose "ports and allow less of a number of bits to be forwarded than were transmitted".

However, Almay discloses a plurality of input ports for successively receiving said data packets (see FIG. 1, two input interfaces to Node B receiving packets) from a respective plurality of routing paths (see FIG. 1, from different/separate paths a-b and A-B; see col. 2, line 33-67; see col. 4, line 20-35); and

an output port for forwarding data packets (see FIG. 1, 3, and output interface of Node B for routing packets; col. 2, line 56 to col. 3, line 50);

wherein in response to a data packet being received at a first of any one of the plurality input ports (see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20), data packets are wait/hold for a period of time at the first input port (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for

predetermined period) while being allowed at the other input ports (see FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60), thereby allowing less of a number of bits to be forwarded than were transmitted **(see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "ports and allow less of a number of bits to be forwarded than were transmitted", as taught by Almay in the system of Voelker, so that it would minimum loss of data; see Almay col. 1, line 45-50.

Regarding Claim 12, Voelker discloses wherein the data packets are forwarded without the discarded data packets received at the first of the inputs (see Voelker claim 1,4). Almay also discloses ports as set forth above in claim 11.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide ports, as taught by Almay in the system of Voelker, so that it would minimum loss of data; see Almay col. 1, line 45-50.

Regarding Claim 13, Voelker discloses the period of time has a predetermined length of time (see Voelker, claim 1-4). Almay discloses wherein the period of time is a predetermined period of time (see FIG. 2, a time is a predefined period of time; see col. 3, line 1-15).

Regarding Claim 14, Voelker discloses wherein the period of time is terminated in response to a determination that a data packet condition is no longer possible (see Voelker claim

1, 4). Almay discloses wherein the period of time is terminated in response to a determination that a data packet condition is no longer possible (see FIG. 2, predetermined time period has elapsed/terminated when determining that receiving packet state/condition impossible since the a-b line/path is deactivated; see col. 3, line 10-30

Regarding Claim 15, Voelker discloses discard data packets for a period of time at all input ports apart from a single input where data packets are determined to be arriving in the correct order (see claim 1-4).

Regarding Claim 16, Voelker discloses wherein only data packets the single input where data packets are determined to be arriving in the correct order are forwarded (see claim 1-4).

4. Claims 5 and 10 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1-4 of U.S. Patent No. 6,370,112 (hereinafter refers to as Voelker) in view of Almay (US 5,809,011) and further in view of Merchant (US006535489B1).

Regarding Claims 5 and 10, the combined system of Voelker and Almay discloses the communication network as set forth above in claims 1 and 6.

Neither Voelker nor Almay explicitly disclose an Ethernet Network.

However, utilizing Ethernet 802.3 network is well known in the art in order to provide a standard connection for interoperability. In particular, Merchant discloses an Ethernet network (see FIG. 1, Ethernet 802.3 network; see col. 3, line 45-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide Ethernet network, as taught by Merchant, in the combined

system of Voelker and Soirinsuo, so that it would enable selectively forwarding data packets to appropriate destination based on Ethernet protocol; see Merchant col. 3, line 60-65.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 6 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Boduch (US006667954B1).

Regarding Claim 1, Boduch discloses a communication network (see FIG. 1, redundant switching system 100), comprising:

at least two mutually different routing paths for commonly sourcing data packets (see FIG. 1, first path 105-111 and second path 106-112 for common source cells 103; see col. 3, line 36-67);

a switch (see FIG. 1, 2, Cell stream alignment best cell copy selection ASIC 100) having a plurality of inputs (see FIG. 1, received/input interfaces for paths 105-111 and 106-112) respectively coupled to the routing paths for receiving the data packets (see FIG. 1, coupling to paths 105-111 and 106-112 for receiving packets/cells; see col. 4, line 1-40,44-53), and an output

for forwarding the data packets (see FIG. 1, transmit/output interface of ASIC 100 for transmitting/forwarding the packets/cells; see col. 4, line 1-40,44-53);

the switch configured to discard or accept data packets depends on the source from which the data packet originate (**see FIG. 1, 2, discarding or transmitting/accepting packets/cells based/depends on the source/originator (*where the packets/cells originate*) (i.e. based on the source/originator who transmit a sequence number and identification number of the packet/cell which is used for discarding/transmitting; see col. 5, line 9-30, 50-65; see col. 6, line 30-60; see col. 8, line 40-50**);

wherein in response to a data packet being received out of order at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets out of sequence at the first receive/input interface 111; see col. 5, line 60 to col. 6, line 7), data packets received at the first input port are discarded for a period of time (see FIG. 2, sequence manager of AISC 110 drops the packet/cell, (e.g. by not writing into FIFO 204, or determining as bad cell), for that period of time; see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40) while data packets received at the other input ports are processed (see FIG. 1,2, while/when receiving packets/cells at the second receive/input interface 112 by writing them into FIFO 204 for transmission; see col. 6, line 20-29,60 to col. 7, line 5, see col. 7, line 20-30; see col. 10, line 32 to col. 11, line 6) such that the data packets forwarded on the output are in correct order (see FIG. 1,2, so that packets/cells transmitted from the cell selector 206 at output/transmit interface of ASIC 100 is sequential order; see col. 10, line 32 to col. 11, line 6) and further allow less of a number of bits to be forwarded than were transmitted (see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56;

see col. 7, line 7-15, 33-44; see col. 8, line 35-40; allowing/selecting best copy of cell bits (note that ATM cell is 53 bytes/424 bits) for forwarding at the output/transmit interface than transmitted from input interface by discarding/dropping "not receiving" bad/out-of-sequence/copied cell bits thereby allowing/selecting the less number of cell bits to be transmitted; in other word, discarding cause the less number of cells/bits to be forwarded/allowed/selected than originally transmitted packets).

Regarding Claim 6, Boduch discloses a switch (see FIG. 1, 2, Cell stream alignment best cell copy selection ASIC 100) for use in a communication network (see FIG. 1, redundant switching system 100), the switch receiving data packets having a packet order (see FIG. 1,2, receiving packets/cells in a sequential order; see col. 4, line 1-40,44-53), determining whether the received data packets are in correct order (see FIG. 1, 2, determine/checking whether the received packets/cells are in a sequential order), and forwarding the received data packets in correct packet order (see FIG. 1, 2, transmitting/forward the received packet/cell in a proper sequential order; see col. 10, line 32 to col. 11, line 6), the switch comprising:

at least two incoming ports for receiving data packets (see FIG. 1, received/input interfaces/ports for paths 105-111 and 106-112 for receiving packets/cells) via respective routing paths (see FIG. 1, via paths 105-111 and 106-112; see col. 4, line 1-40,44-53) and an output port for forwarding data packets (see FIG. 1, transmit/output interface of ASIC 100 for transmitting/forwarding the packets/cells; see col. 4, line 1-40,44-53);

said data packets are discarded or accepted depending on the source form which the data packet originate (**see FIG. 1, 2, discarding or transmitting/accepting packets/cells based/depends on the source/originator (*where the packets/cells originate*) (i.e. based on the**

source/originator who transmit a sequence number and identification number of the packet/cell which is used for discarding/transmitting; see col. 5, line 9-30, 50-65; see col. 6, line 30-60; see col. 8, line 40-50);

wherein in response to a commonly sourced data packet being received out of order at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets out of sequence at the first receive/input interface 111; see col. 5, line 60 to col. 6, line 7), commonly sourced data packets received at the first input port are discarded for a period of time (see FIG. 2, sequence manager of AISC 110 drops the packet/cell, (e.g. by not writing into FIFO 204, or determining as bad cell) while commonly sourced data packets received at the other input ports are processed (see FIG. 1,2, while/when receiving packets/cells at the second receive/input interface 112 by writing them into FIFO 204 for transmission; see col. 6, line 20-29,60 to col. 7, line 5, see col. 7, line 20-30; see col. 10, line 32 to col. 11, line 6) thereby allow less of a number of bits to be forwarded than were transmitted (see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40; allowing/selecting best copy of cell bits (note that ATM cell is 53 bytes/424 bits) for forwarding at the output/transmit interface than transmitted from input interface by discarding/dropping "not receiving" bad/out-of-sequence/copied cell bits thereby allowing/selecting the less number of cell bits to be transmitted; in other word, discarding cause the less number of cells/bits to be forwarded/allowed/selected than originally transmitted packets).

Regarding Claim 11, Boduch discloses a switch (see FIG. 1, 2, Cell stream alignment best cell copy selection ASIC 100) for use in a communication network (see FIG. 1, redundant switching system 100), the switch receiving data packets having a packet order (see FIG. 1,2,

receiving packets/cells in a sequential order; see col. 4, line 1-40,44-53), determining whether the received data packets are in correct order (see FIG. 1, 2, determine/checking whether the received packets/cells are in a sequential order), and forwarding the received data packets in correct packet order (see FIG. 1, 2, transmitting/forward the received packet/cell in a proper sequential order; see col. 10, line 32 to col. 11, line 6), comprising:

a plurality of input ports for successively receiving said data packets (see FIG. 1, received/input interfaces/ports for paths 105-111 and 106-112 for receiving packets/cells) from a respective plurality of routing paths (see FIG. 1, via paths 105-111 and 106-112; see col. 4, line 1-40,44-53); and

an output port for forwarding data packets (see FIG. 1, transmit/output interface of ASIC 100 for transmitting/forwarding the packets/cells; see col. 4, line 1-40,44-53);

said data packets are discarded or accepted depending on the source form which the data packet originate (**see FIG. 1, 2, discarding or transmitting/accepting packets/cells based/depends on the source/originator (*where the packets/cells originate*) (i.e. based on the source/originator who transmit a sequence number and identification number of the packet/cell which is used for discarding/transmitting; see col. 5, line 9-30, 50-65; see col. 6, line 30-60; see col. 8, line 40-50**);

wherein in response to a data packet being received out of order at a first of any one of the plurality input ports (see FIG. 1,2, after receiving cells/packets out of sequence at the first receive/input interface 111; see col. 5, line 60 to col. 6, line 7), data packets are discarded for a period of time at the first input port (see FIG. 2, sequence manager of AISC 110 drops the packet/cell, (e.g. by not writing into FIFO 204, or determining as bad cell)) while being allowed

at the other input ports (see FIG. 1,2, while/when receiving packets/cells at the second receive/input interface 112 by writing them into FIFO 204 for transmission; see col. 6, line 20-29,60 to col. 7, line 5, see col. 7, line 20-30; see col. 10, line 32 to col. 11, line 6) and thereby allowing less of a number of bits to be forwarded than were transmitted (see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40; allowing/selecting best copy of cell bits (note that ATM cell is 53 bytes/424 bits) for forwarding at the output/transmit interface than transmitted from input interface by discarding/dropping "not receiving" bad/out-of-sequence/copied cell bits thereby allowing/selecting the less number of cell bits to be transmitted; in other word, discarding cause the less number of cells/bits to be forwarded/allowed/selected than originally transmitted packets).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4, 6-9, and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Almay (US005809011A) in view of Soirinsuo (US006028861A).

Regarding Claim 1, Almay discloses a communication network (see FIG. 1, packet switch communication network), comprising:

at least two mutually different routing paths for commonly sourcing data packets (see FIG. 1, different/separate paths a-b and A-B for transmission of packets from common source node A (i.e. common souring data packets) since both paths a-b and A-B have common source Node A; see col. 2, line 33-50, see col. 3, line 10-26); and

a switch (see FIG. 1, Node B) having a plurality of inputs (see FIG. 1, received/input interfaces a-b and A-B) respectively coupled to the routing paths for receiving the data packets (see FIG. 1, coupling to a-b path and another interface from A-B path for receiving packets; see col. 2, line 38-67; see col. 4, line 20-35), and an output for forwarding the data packets (see FIG. 1, transmit/output interface of Node B for transmitting/forwarding the packets; see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50);

the switch configured to perform processing data packet depending on the source from which the data packets originate (**see FIG. 1, Node B performing processing of packets depending/based on the source node A, where node A transmits packet at different time or Node A transmit re-route notification; see col. 3, line 1-60**);

wherein in response to a data packet being received at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20), data packets received at the first input port are wait/hold for a period of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for predetermined period) while data packets received at the other input ports are processed (see FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60) such that the data packets forwarded on the output are in correct order (see FIG. 1,

routing the received packet in a correct/proper order (i.e. note that a correct/proper order of packets is formed when nodes A and B deactivating the route a-b for a predetermined time then activating the route A-B) via an output interface of node B; see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50).

Almay does not explicitly disclose "out of order", "discard or accept" data packets, and "allow less of a number of bits to be forwarded than were transmitted".

However, receiving packets/cells/frames out of order due to changing network condition such as unavailable/fail/congested path and discarding the discarding out of order cells packets/cells/frames received at the port/interface in order to maintain network integrity is so well know in the art. In particular, Soirinsuo teaches a switch (see FIG. 8, 11, Switch) having a plurality of inputs for receiving the data packets (see FIG. 8, 11, input channels ports 1104 for receiving cells/packets), and an output for forwarding the data packet (see FIG. 8, 11, output channel port 1106 for route/forward the packets/cells; see col. 9, line 20-35; see col. 10, line 29-46);

the switch configured to discard or accept data packet depending on the source from which the data packets originate (**see FIG. 8, 9, 11, discarding or forwarding packets/cells depends/based on the originator/source switch who sends packets with last cell indication set (i.e. AUU or signaling) with associated cell identification VPI/VCI; last cell indication set cause the switchover to discard, non-last cell indication does not cause the switchover; see col. 9, line 1-30, 50-65; see col. 10, line 5-25**);

wherein in response to a data packet being received out of order at a first of the plurality input ports (see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the

same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the first normal input port of 1104; see col. 9, line 20-35), data packets received at the first input port are discarded for a period of time (see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the first/normal/old channel port 1104 are discarded during switch-over interval/time) while data packets received at the other input ports are processed (see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new channel port), such that the data packets forwarded on the output are in correct packet order (see FIG. 8, 11, the packets/cells are transmitted/forwarded on the output channel port 1106 in the same proper/accurate order (i.e. the order as if the packets/cells are not lost due to failure/congestion); see col. 9, line 20-35; see col. 10, line 29-46) and further allow less of a number of bits to be forwarded than were transmitted (see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "discard or accept, out of order and allow less of a number of bits to be forwarded than were transmitted", as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 2, the combined system of Almay and Soirinsuo discloses all claimed limitations. In particular, Almay discloses in response to a commonly sourced data packet being received at a second of the plurality input ports (see FIG. 2, when receiving packets/cells at the

second interface A-B; see col. 3, line 1-60), commonly sourced data packets received at all of the input ports are hold/wait for a period of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing packets/cells at the first interface a-b or other interfaces (since ATM node can have more than two interfaces, see Almay col. 5, line 1-16; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20).

Soirinsuo teaches in response to a commonly sourced data packet being received out of order at a second of the plurality input ports (see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the second normal input port of 1104; see col. 9, line 20-35), commonly sourced data packets received at all of the input ports are discarded for a period of time (see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the second/normal/old channel port 1104 are discarded during switch-over interval/time) while commonly sourced data packets received at the other input ports are processed (see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new/first channel port).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide discarding and out of order, as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 3, Almay discloses the period of time lasts until the switch is informed that re-ordering of the commonly sourced data packets is no longer possible (see col. 3, line 1-50; predefined period is defined such that ordering of packets at the new route connection that transmit cells/packets from possible and not disrupted. Since the predefined time last until the

"ordering" of packet is "possible/not-disrupted", and thus "re-ordering" of packets are "not possible/disrupted").

Regarding Claim 4, Almay discloses the period of time has a predetermined length of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing packets/cells from subscriber A at the first interface a-b for predetermined period). Soirinsuo also discloses the period of time has a predetermined length of time (see FIG. 8, 11, first/normal connection/port; see col. 9, line 40-45; see col. 10, line 10-30; discarding all cells received from first/normal connection/port from the input source during switch-over interval/time).

Regarding Claim 6, Almay discloses a switch (see FIG. 1, 3, Node B) for use in a communication network (see FIG. 1, packet switch communication network), the switch receiving data packets having a packet order (see FIG. 1,3, receiving packets in a correct/proper order of packets), determining whether the received data packets are in correct order (see FIG. 1, 3, determine/checking whether the received packets are in a correct/proper order), and forwarding the received data packets in correct packet order (see FIG. 1, 3, routing/forward the received packet from source node A in a correct/proper order (i.e. note that a correct/proper order of packets is formed when nodes A and B deactivating the route a-b for a predetermined time then activating the route A-B); see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50), the switch comprising:

at least two incoming ports for receiving data packets (see FIG. 1, two input interfaces to Node B receiving packets) via respective routing paths (see FIG. 1, via different/separate paths a-b and A-B; see col. 2, line 33-67; see col. 4, line 20-35) and an output port for forwarding data

packets (see FIG. 1, 3, and output interface of Node B for routing packets; col. 2, line 56 to col. 3, line 50);

said data packets are processed depending on the source from which the data packet originate (**see FIG. 1, Node B performing processing of packets depending/based on the source node A, where node A transmits packet at different time or Node A transmit re-route notification; see col. 3, line 1-60**);

wherein in response to a commonly sourced data packet being received at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20), commonly sourced data packets received at the first input port are wait/hold for a period of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for predetermined period) while commonly sourced data packets received at the other input ports are processed (see FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60).

Almay does not explicitly disclose “out of order”, “discard or accept” data packets, “allow less of a number of bits to be forwarded than were transmitted".

However, receiving packets/cells/frames out of order due to changing network condition such as unavailable/fail/congested path and discarding the discarding out of order cells packets/cells/frames received at the port/interface in order to maintain network integrity is so well know in the art. In particular, Soirinsuo teaches a switch (see FIG. 8, 11, Switch) comprising at least two incoming ports for receiving the data packets (see FIG. 8, 11, the input channels ports 1104 for receiving cells/packets) and an output port for forwarding data packets

(see FIG. 8, 11, output channel port 1106 for routing cells/packets; see col. 9, line 20-35; see col. 10, line 29-46);

said data packets are discarded or accepted depending on the source from which the data packet originate (**see FIG. 8, 9, 11, discarding or forwarding packets/cells depends/based on the originator/source switch who sends packets with last cell indication set (i.e. AUU or signaling) with associated cell identification VPI/VCI; last cell indication set cause the switchover to discard, non-last cell indication does not cause the switchover; see col. 9, line 1-30, 50-65; see col. 10, line 5-25);**

wherein in response to a commonly sourced data packet being received out of order at a first of the plurality input ports (see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the first normal input port of 1104; see col. 9, line 20-35), commonly sourced data packets received at the first input port are discarded for a period of time (see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the first/normal/old channel port 1104 are discarded during switch-over interval/time) while commonly sourced data packets received at the other input ports are processed (see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new channel port), thereby allowing less of a number of bits to be forwarded than were transmitted (see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "discard or accept, out of order, allow less of a number of bits to be forwarded than were transmitted", as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 11, Almay discloses a switch (see FIG. 1, 3, Node B) configured for receiving data packets having a packet order (see FIG. 1,3, receiving packets in a correct/proper order of packets), determining whether the received data packets are in correct order (see FIG. 1, 3, determine/checking whether the received packets are in a correct/proper order), and forwarding the received data packets in correct packet order (see FIG. 1, 3, routing/forward the received packet from source node A in a correct/proper order (i.e. note that a correct/proper order of packets is formed when nodes A and B deactivating the route a-b for a predetermined time then activating the route A-B); see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50), comprising:

a plurality of input ports for successively receiving said data packets (see FIG. 1, two input interfaces to Node B receiving packets) from a respective plurality of routing paths (see FIG. 1, from different/separate paths a-b and A-B; see col. 2, line 33-67; see col. 4, line 20-35); and

an output port for forwarding data packets (see FIG. 1, 3, and output interface of Node B for routing packets; col. 2, line 56 to col. 3, line 50);

said data packets are processed depending on the source from which the data packet originate (**see FIG. 1, Node B performing processing of packets depending/based on the**

source node A, where node A transmits packet at different time or Node A transmit re-route notification; see col. 3, line 1-60);

wherein in response to a data packet being received at a first of any one of the plurality input ports (see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20), data packets are wait/hold for a period of time at the first input port (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for predetermined period) while being allowed at the other input ports (see FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60).

Almay does not explicitly disclose "out of order", "discard or accept", "allow less of a number of bits to be forwarded than were transmitted".

However, receiving packets/cells/frames out of order due to changing network condition such as unavailable/fail/congested path and discarding the discarding out of order cells packets/cells/frames received at the port/interface in order to maintain network integrity is so well know in the art. In particular, Soirinsuo teaches a switch (see FIG. 8, 11, Switch) comprising a plurality of input ports for successively receiving said data packets (see FIG. 8, 11, the input channels ports 1104 for receiving cells/packets); and

an output port for forwarding data packets (see FIG. 8,11, output channel port 1106 for routing cells/packets; see col. 9, line 20-35; see col. 10, line 29-46);

said data packets are discarded or accepted depending on the source from which the data packet originate (**see FIG. 8, 9, 11, discarding or forwarding packets/cells depends/based on the originator/source switch who sends packets with last cell indication set (i.e. AUU or**

signaling) with associated cell identification VPI/VCI; last cell indication set cause the switchover to discard, non-last cell indication does not cause the switchover; see col. 9, line 1-30, 50-65; see col. 10, line 5-25);

wherein in response to a data packet being received out of order at a first of any one of the plurality input ports (see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the first normal input port of 1104; see col. 9, line 20-35), data packets are discarded for a period of time at the first input port (see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the first/normal/old channel port 1104 are discarded during switch-over interval/time) while being allowed at the other input ports (see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new channel port), thereby allowing less of a number of bits to be forwarded than were transmitted (**see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "discard or accept, out of order, allow less of a number of bits to be forwarded than were transmitted", as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 7, the claim, which has disclosed all the limitations of the respective claim 2. Therefore, it is subjected to the same rejection as set forth above in claim 2.

Regarding Claim 8, the claim, which has disclosed all the limitations of the respective claim 3. Therefore, it is subjected to the same rejection as set forth above in claim 3.

Regarding Claim 9, the claim, which has disclosed all the limitations of the respective claim 4. Therefore, it is subjected to the same rejection as set forth above in claim 4.

Regarding Claim 12, Soirinsuo discloses wherein the data packets are forwarded without the discarded data packets received at the first of the input ports (see FIG. 8, 11, packets/cells are routed/forwarded without discarded cells/packets received at the first input channel port 1104; note that since the received packets/cells are discarded at the first input channel port 1104, and thus the discarded packets/cells are not forward/routed; see col. 10, line 25-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the data packets are forwarded without the discarded data packets received at the first of the input ports, as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 13, Almay discloses wherein the period of time is a predetermined period of time (see FIG. 2, a time is a predefined period of time; see col. 3, line 1-15).

Regarding Claim 14, Almay discloses wherein the period of time is terminated in response to a determination that a data packet condition is no longer possible (see FIG. 2, predetermined time period has elapsed/terminated when determining that receiving packet state/condition impossible since the a-b line/path is deactivated; see col. 3, line 10-30). Soirinsuo also discloses wherein the period of time is terminated in response to a determination that a data

packet condition is no longer possible (see col. 10, line 25-30; the switch-over interval/time is terminated/ended after all packets/cells are discarded which causes the packet status/condition no longer possible).

Regarding Claim 15, Soirinsuo discloses discard data packets for a period of time at all input ports apart from a single input (see col. 9, line 40-45; see col. 10, line 10-30; discarding all cells for a switch-over interval/time at the first/normal/old channel port 1104 apart from the second/new input channel port 1104) where data packets are determined to be arriving in the correct order (see FIG. 8, where cells/packets are received in the same order in which they are transmitted (i.e. correct order); see col. 9, line 20-35, 40-45; see col. 10, line 10-30).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide discarding data packets for a period of time at all input ports apart from a single input where data packets are determined to be arriving in the correct order, as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 16, Soirinsuo discloses wherein only data packets the single input where data packets are determined to be arriving in the correct order are forwarded (see col. 9, line 40-45; see col. 10, line 10-30; cell/packets in the new/second input channel where cells/packets are receiving/arriving in the same order in which they are transmitted (i.e. correct order) are forwarded/routed).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide only data packets the single input where data packets are determined to be arriving in the correct order are forwarded, as taught by Soirinsuo in the system

of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

9. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Almay in view of Soirinsuo as applied to claims 1 and 6 above, and further in view of Merchant (US006535489B1).

Regarding Claims 5 and 10, the combined system of Almay and Soirinsuo discloses the communication network as set forth above in claims 1 and 6.

Neither Almay nor Soirinsuo explicitly disclose "an Ethernet Network".

However, utilizing Ethernet 802.3 network is well known in the art in order to provide a standard connection for interoperability. In particular, Merchant discloses an Ethernet network (see FIG. 1, Ethernet 802.3 network; see col. 3, line 45-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide Ethernet network, as taught by Merchant, in the combined system of Almay and Soirinsuo, so that it would enable selectively forwarding data packets to appropriate destination based on Ethernet protocol; see Merchant col. 3, line 60-65.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IAN N. MOORE whose telephone number is (571)272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derrick W. Ferris can be reached on 571-272-3123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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